REMARKS

In the Official Action mailed on **19 May 2006**, the Examiner reviewed claims 1-21. Claims 1-4, 6-14, and 16-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nguyen et al (USPN 5,887,275, hereinafter "Nguyen"), in view of Mattis et al (USPN 6,128,623, hereinafter "Mattis"). Claims 5 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nguyen, in view of Mattis, and further in view of Malcolm (USPN 6,427,187, hereinafter "Malcolm").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 11, and 21 were rejected as being unpatentable over Nguyen, in view of Mattis. Applicant respectfully points out that the combined system of Nguyen and Mattis teaches **a software system** for caching database entries and web pages in memory (see Nguyen, col. 5, lines 58-61 and Mattis, col. 7, lines 52-65).

In contrast, the present invention incorporates **a hardware translator** in a central processing unit that translates between object identifiers (used to reference objects in an object cache within the CPU) and physical addresses (used to address objects in main memory). This is beneficial because it provides faster execution than a software based solution. The systems of Nguyen and Mattis will typically cause the CPU to stall while waiting for the software system to respond. There is nothing within Nguyen or Mattis, either separately or in concert, which suggests incorporating a hardware translator at a central processing unit to translate between object identifiers and physical addresses.

Furthermore, it is not obvious to build such a hardware translator, because, for performance reasons, the translator needs to be coupled to a separate memory containing object table entries, and furthermore, for performance reasons the best place to locate the translator is between L2 cache and memory, not further up the

memory hierarchy. These design decisions that make the hardware translator practical are not obvious.

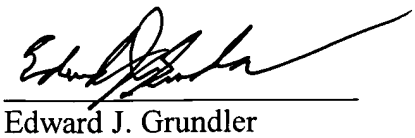
Accordingly, Applicant has amended independent claims 1, 11, and 21 to clarify that the present invention incorporates a hardware translator within a central processing unit to translate between object identifiers and physical addresses. These amendments find support in FIG. 1 and paragraphs [0027]-[0030]. Dependent claims 2 and 12 have been canceled without prejudice. Dependent claims 3 and 13 have been amended to correct antecedent basis.

Hence, Applicant respectfully submits that independent claims 1, 11, and 21 as presently amended are in condition for allowance. Applicant also submits that claims 3-10, which depend upon claim 1, and claims 13-20, which depend upon claim 11, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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